✆ STD - 0431 - 2670142
FAX - 0431 - 2670143

DHANALAKSHMI SRINIVASAN
INSTITUTE OF TECHNOLOGY
(Approved by AICTE, New Delhi & Affiliated to Anna University)
NH - 45, Trichy - Chennai Trunk Road,
SAMAYAPURAM,TRICHY - 621 112.
E.mail:dsit2011@gmail.com Website:www.dsit.ac.in

COURSE PLAN

Subject code: EC8095	**Branch/Year/Sem/Section: B.E ECE/III/VI**
Subject Name: VLSI DESIGN	**Batch:2017-2021**
Staff Name:R.KEERTHIGA	**Academic year:2019-2020**

COURSE OBJECTIVE

1. Study the fundamentals of CMOS circuits and its characteristics.
2. Learn the design and realization of combinational & sequential digital circuits.
3. Architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology are discussed.
4. Learn the different FPGA architectures and testability of VLSI circuits.

TEXT BOOK:

1. Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective‖, 4th Edition, Pearson , 2017 (UNIT I,II,V)

2. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective‖, Second Edition , Pearson , 2016.(UNIT III,IV)

REFERENCES:

1. M.J. Smith, —Application Specific Integrated Circuits‖, Addisson Wesley, 1997
2. Sung-Mo kang,Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition ,2013
3. Wayne Wolf, —Modern VLSI Design: System On Chip‖, Pearson Education, 2007
4. R.Jacob Baker, Harry W.LI., David E.Boyee, —CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.

WEB RESOURCES

W1: www.srmuniv.ac.in/openware_d_loads/u2L4.ppt
W2 :http://cc.ee.ntu.edu.tw/~thc/course_mckt/note/note2.pdf
W3: www.cdeep.iitb.ac.in/nptel/Electrical%20…/Lec25(m4).html

TEACHING METHODOLOGIES:

- BB - BLACK BOARD
- PPT - POWER POINT PRESENTATION

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC8095	**VLSI DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

UNIT I INTRODUCTION TO MOS TRANSISTOR 9

MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.

UNIT II COMBINATIONAL MOS LOGIC CIRCUITS 9

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls.

Power: Dynamic Power, Static Power, Low Power Architecture.

UNIT III SEQUENTIAL CIRCUIT DESIGN 9

Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits.

Timing Issues : Timing Classification Of Digital System, Synchronous Design.

UNIT IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM 9

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study:Design as a tradeoff.

Designing Memory and Array structures:Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

UNIT V IMPLEMENTATION STRATEGIES AND TESTING 9

FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

TOTAL: 45 PERIODS

Topic No	Topic Name	Books For reference	Page No	Teaching Methodology	No of periods required	Cumulative periods
UNIT I	**UNIT I- MOS TRANSISTOR PRINCIPLE**				**(9)**	
1.	NMOS and PMOS transistors	R1	05	BB	2	1
2.	Process parameters for MOS and CMOS	R1	45,	BB	1	2
3.	Electrical properties of CMOS circuits and device modeling	R1	51	BB	1	3
4.	Scaling principles and fundamental limits	R1	54	BB	1	4
5.	CMOS inverter	R1	18	BB	2	5
6.	Scaling & propagation delays	R1	20	BB	1	6
7.	Layout diagrams	R1	24	BB	1	7
8.	Stick diagram,	R1	26	BB	2	8
9.	Elmore's constant	T2	292	BB	2	9
LEARNING OUTCOME: **At the end of unit , the students will be able to** • Understand the MOS transistor.						
UNIT II		**(9)**				
10.	Examples of Combinational Logic Design	R1	215	BB	1	10
11.	Static CMOS design	R1	216	BB	2	11
12.	Pass transistor Logic	R1	232	BB	1	12
13.	Transmission gates	T2	280	BB	1	13
14.	Dynamic CMOS design	R1	216	BB	2	14

15.	Power dissipation	R1	228	BB,	1	15
16.	Low power design principles	T1	242	BB	1	16
17.	Static power dissipation	T1	246	BB	1	17
18.	Dynamic power dissipation	T1	244	BB	1	18

LEARNING OUTCOME:

At the end of unit , the students will be able to

- Understand the concept of combinational circuits
- Power dissipation

UNIT-III-	**SEQUENTIAL LOGIC CIRCUITS**					**(9)**
19.	Static and Dynamic Latches	R7	396	BB	1	19
20.	Registers, Pulse registers	R7	398	BB	1	20
21.	Timing issues, pipelines	R7	404-406	BB	1	21
22.	Sense amplifier based register	T1	287	BB	1	22
23.	clock strategies	R7	415	BB	1	23
24.	Memory architecture and memory control circuits	R7	424	BB	2	24
25.	Low power memory circuits	R7	431	BB	1	25
26.	Synchronous sequential circuits	R7	441	BB	1	26
27.	Asynchronous design circuits	R7	443	BB	1	27

LEARNING OUTCOME:

At the end of unit , the students will be able to

- Understand the concept of static and dynamic circuits.

UNIT-IV-	**DESIGNING ARITHMETIC BUILDING BLOCKS**				**(9)**	
28.	Data path circuits	T2	166	BB	1	28
29.	Architectures for ripple carry adders	R1	303	BB	1	29
30.	carry look ahead adders	R1	304	BB	1	30
31.	High speed adders, Accumulators	R1	329	BB	1	31

32.	Memory architecture, memory peripheral circuitry	T1	318	BB	1	32
33.	Multipliers & dividers	R1	345	BB	2	33
34.	Barrel shifters	R1	343	BB	1	34
35.	Design tradeoff	R1	346	BB	1	35
36	Speed and area tradeoff	R1	363	BB	1	36

LEARNING OUTCOME:

At the end of unit , the students will be able to

- Understand the concept adders,multipliers
- Barrel shifters

UNIT-V-	**IMPLEMENTATION STRATEGIES**					**(9)**
37.	Full custom and Semi custom design	T2	313	BB	1	37
38.	Standard cell design and cell libraries	T2	344	BB	1	38
39.	FPGA building block architectures	T2	319	BB	1	39
40.	FPGA interconnect routing	T2	923	BB	1	40
41.	Design for testability	T1	401	BB	1	41
42.	Adhoc-testing	T1	408	BB	1	42
43.	BIST,IDDQ testing	T1	412	BB	1	43
44.	Scan design,boundary scan	T1	416	BB	1	44
45.	Design for manufacturability	T1	417	BB		45

LEARNING OUTCOME:

At the end of unit , the students will be able to

- FPGA and ASIC

COURSE OUTCOME

At the end of the course, the student should be able to:

- characteristics of MOS transistor and fabrication techniques
- Knowledge about the combinational and sequential circuit functions.
- Capable to work with Xilinx software

CONTENT BEYOND THE SYLLABUS

ALTERA Quaratus 9.1

CONTINUES INTERNAL ASSESSMENT DETAILS

ASSESMENT NUMBER	I	II	MODEL
TOPIC NO.(UNIT)	1-18 (1st & 2nd units)	19-36 (3rd & 4th units)	1-45 (units 1-5)

ASSIGNMENT DETAILS

ASSIGNMENT NUMBER	I	II	III
TOPIC NUMBER FOR REFERENCE	1-18 (1st & 2nd units)	19-36 (3rd & 4th units)	1-45 (units 1-5)
DEAD LINE			

ASSIGNMENT NUMBER	BATCH	DESCRIPTIVE QUESTIONS/TOPIC (Minimum of 8 Pages)
I	B1	1. Nmos transistor 2. Fabrication techniques 3. Cmos design circuits
II	B1	1. Examples of combinational circuits 2. Pass transistor logic 3. Design multiplexer with transmission gates.
III	B1	1. FPGA Architectures 2. Xilinx functions 3. ASIC implementations

PREPARED BY **VERIFIED BY**

R.KEERTHIGA, AP/ECE **HOD/ECE**

APPROVED BY

PRINCIPAL